REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached marked-up version is captioned "Version with markings to show changes made."

Claims 28 – 50 are pending in the application.

Claim 28 has been amended. A new independent claim 50 has been added.

Applicants thank the Examiner and his supervisor for the opportunity on March 13, 2003 to discuss the present application. During that discussion, Applicants proposed amendments to claim 28 and it was agreed that Applicants would submit, via an amendment, an amended claim 28 for entry in the record and that Applicants would point out the distinguishing features of the method as recited in amended claim 28.

In the Office Action, claims 28 - 35, 37, 38, and 44 - 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,967,794 to Kodama. Additionally, in the Office Action, claims 36, 39, 41, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,967,794 to Kodama as applied to claims 28 - 35, 37, 38, and 44 - 49 and further in view of the Wolf et al reference. Applicants respectfully submit that claim 28 as now amended patentably defines over Kodama and Wolf et al and submit that claim 28, and claims 29 - 49 depending ultimately therefrom, and new independent claim 50, are in condition for allowance.

Claim 28 as now amended recites a method of generating defects in a lattice

structure of a semiconductor material during thermal treatment of the material. The method includes subjecting the semiconductor material to a treatment protocol comprising a preliminary step and a later step which occurs after the preliminary step. The preliminary step includes controlling at least one of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere such that the subsequent concentration and diffusion of foreign atoms within the semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in the semiconductor material. Also, in accordance with the method recited in amended claim 28 of the present application, the later step of the treatment protocol includes either producing an $Si_xO_yN_z$ oxy-nitride layer having a thickness of up to 2nm (20 angstroms) on a surface of the semiconductor material or producing an Si_3N_4 layer having a thickness of up to 4nm (40 angstroms) on the semiconductor material at a location on the surface of said semiconductor material at which a natural SiO_2 layer has previously been removed prior to the thermal treatment of the semiconductor material.

The defects in the lattice structure generated by the method recited in amended claim 28 can include, as recited in claim 29, so-called vacancies or, as recited in claim 30, semiconductor substrate atoms on interstitial lattice positions. The defects that are produced influence the diffusion characteristics of foreign atoms within the semiconductor material.

Kodama discloses a method of making a semiconductor device with a shallow PN junction depth on the order of 50 nm. In order to now provide a flat PN junction

depth, Kodama first selectively applies a silicon layer (raised layer) in that region in which a flat PN junction is to be formed; such a silicon layer (raised layer) contains carbon or nitrogen, the purpose of which is to combine with the point defects and thus prevent a defect enhanced diffusion (see column 4, first paragraph of Kodama). After the application of the silicon layer, foreign atoms are implanted into the applied layer via ion implantation. During a subsequent thermal treatment of the substrate, the foreign atoms diffuse into the applied layer and into the substrate disposed below the layer, and in particular pursuant to Kodama to a depth of 100 nm from the surface of the applied layer.

It is respectfully submitted that Kodama neither teaches nor suggests the treatment protocol including the preliminary step and the later step which occurs after the preliminary step as recited in amended claim 28 of the present application. Specifically, it can be seen that Kodama provides no teaching nor suggestion concerning such a two-step treatment protocol in which the preliminary step includes controlling at least one of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere such that the <u>subsequent</u> concentration and diffusion of foreign atoms within the semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in the semiconductor material. Instead, Kodama discloses, as part of its step of selectively growing a "raised' semiconductor layer, that such a "raised' semiconductor layer contains, as set forth in Col. 4, lines 6 - 9 of Kodama, "a substance such as carbon which tends to combine with point defects in the

semiconductor substrate and/or a substance such as nitrogen which prevents a dopant impurity from diffusing."

Kodama further teaches, in Col. 4, lines 20 -21 thereof, that, since the substance such as carbon and/or nitrogen "is introduced into the selectively grown, raised layer not by ion-implantation but during the growth of the raised layer, <u>there is no residual defects formed</u>." Once the selectively grown raised layer of Kodama - which is described in the specification of Kodama as the raised layer 6B - has been grown, then BF_2 is ion implanted and the semiconductor substrate is subjected to thermal treatment. See, for example, Col. 5, lines 31 - 40 of Kodama: "In order to obtain the distribution of boron concentration within the raised layer 6B as shown in FIG. 2(a), BF_2 is ion implanted in the raised layer 6B with injection energy of 10 to 20 keV and with a dose of 2×10^{15} atoms/cm^3. Then, the implanted boron is activated and diffused into the underlying substrate by annealing the wafer in nitrogen atmosphere at 800 degrees C. for about 10 minutes in a heat-treatment furnace, resulting in a source/drain region 9 having the raised layer 6B with a concentration distribution such as shown in FIG. 2(b)."

Thus, it can be seen that Kodama provides no disclosure or teaching of the particular preliminary and later steps of the two step treatment protocol recited in claim 28 as now amended. Specifically, Kodama does not disclose nor teach that the annealing of its semiconductor substrate results in a diffusion of foreign atoms into the semiconductor substrate such that, in the language of amended claim 28, "the subsequent concentration and diffusion of foreign atoms within said

semiconductor material are influenced by the <u>newly created</u> respective concentration or distribution of defects or vacancies in said semiconductor material". This is because the Kodama process does not contemplate the creation of new defects in the semiconductor substrate. Instead, in the Kodama process, to the extent that carbon is the substance introduced into the raised layer 6B during its selective growth, the carbon will tend to combine with (already existing) point defects in the semiconductor substrate. Thus, it can be readily understood that Kodama provides no teaching concerning a two step treatment protocol having a preliminary step involving control of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere such that the subsequent concentration and diffusion of foreign atoms within the semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in the semiconductor material since, as noted, Kodama does not contemplate the creation of new defects in the semiconductor substrate.

Applicants also submit that Wolf et al likewise provides no teaching or suggestion of the method recited in amended claim 28. Instead, Wolf relates only to the application of various layers upon a semiconductor substrate and does not provide any teaching or disclosure to one of skill in the art concerning, for example, the two-step treatment protocol recited in amended claim 28.

Applicants have also submitted herewith a new independent claim 50 which is likewise submitted to patentably define over the prior art of record.

In view of the foregoing discussion, Applicants respectfully request

reconsideration of the allowability of all of the claims of the instant application. Should the Examiner have any further comments or suggestions, the undersigned would very much welcome a telephone call from him in order to be able to discuss any outstanding issues and to place the application into condition for allowance.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

28. (First Amended) A method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material, said method including the steps of:

subjecting said semiconductor material to a treatment protocol comprising a preliminary step and a later step which occurs after the preliminary step, the preliminary step including controlling at least one of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere such that the subsequent concentration and diffusion of foreign atoms within said semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in said semiconductor material; and

the later step of the treatment protocol including either producing an $Si_xO_yN_z$ oxy-nitride layer having a thickness of up to 2nm (20 angstroms) on a surface of [a] said semiconductor material, or

[prior to a thermal treatment, removing a natural SiO_2 layer from a surface of a semiconductor and] producing an Si_3N_4 layer having a thickness of up to 4nm (40 angstroms) on said semiconductor material at a location on said surface of said semiconductor material at which a natural SiO_2 layer has previously been removed prior to the thermal treatment of said semiconductor material .

50. (New) A method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material, said method

including the steps of:

subjecting said semiconductor material to a treatment protocol comprising a preliminary step and a later step which occurs after the preliminary step, the preliminary step including controlling at least one of a concentration and a distribution of defects or vacancies in the form of a selected one of vacancies (empty lattice positions) and semiconductor- substrate atoms on interstitial lattice positions (self-interstitials) as a function of a process gas atmosphere such that the subsequent concentration and diffusion of foreign atoms within said semiconductor material are influenced by the newly created respective concentration or distribution of defects or vacancies in said semiconductor material; and

the later step of the treatment protocol including either producing an $Si_xO_yN_z$ oxy-nitride layer having a thickness of up to 2nm (20 angstroms) on a surface of said semiconductor material, or

producing an Si_3N_4 layer having a thickness of up to 4nm (40 angstroms) on said semiconductor material at a location on said surface of said semiconductor material at which a natural SiO_2 layer has previously been removed prior to the thermal treatment of said semiconductor material.